08 512505

APPLICATION
for
UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that:
Lizy Kurian John,
residing at 1318 thomasville Circle, Apt. C,
Tampa, County of Hillsborough, State of Florida
a citizen of the United States of America

has invented a new and useful Computer Memory Chip with Field Programmable Memory Cell Arrays (FPMCAs), and Method of Configuring, of which the following is a specification.

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Computer Memory Chip with Field Programmable Memory Cell Arrays (FPMCAs), and Method of Configuring

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a programmable computer memory chip and to a method of dynamically configuring the memory chip to different I/O bus widths.

Description of the Background Art

As shown in Fig. 1, conventional computer random access memory (RAM) chip 10 contains a memory array 12 having memory cells that can each be individually addressed by a row decoder 14 and a column decoder 16 to input or output data by means of I/O circuits 18 and input and output data control circuits 20 and 22, respectively as determined by chip select/write enable logic, generally indicated by numeral 24. Most of these chips 10 organize the memory cells in a matrix fashion and employ a decoding scheme utilizing the row and column decoders 14 & 16. More particularly, approximately one-half the address lines 26 are decoded by the row decoder 14 and the remaining address lines 28 are decoded by the column decoder 16.

For example, a 1Mb (megabits of memory) X 1 (word width of 1) chip has 1048576 cells divided into 1024 rows and 1024 columns. There are 20 address lines, 10 of which are used to

select one of the 1024 rows of memory cells. The remaining 10 bits are used as column address inputs to select one of the 1024 columns. The row decoder 14 has 10 inputs and 1024 outputs. The column decoder also has 10 inputs and 1024 outputs. For any specific address, only one of the 1024 rows and only one of the 1024 columns will be activated, and only one cell gets active row and column address and the output of that cell will appear at the memory output. The I/O circuit 18 permits a stored bit to be output to the data output pin 22 during a read and to be changed by the input 20 from the data during a write. In dynamic RAMs, the I/O circuits 28 will include sense amplifiers, etc.

Several innovative static RAM (SRAM) and dynamic RAM (DRAM) architectures have been proposed recently, examples being fast static RAMs from Motorola such as BurstRAMs and DSPRAMs, the cached DRAM from Mitsubishi and Ramtron, the synchronous DRAM from the Joint Electron Devices Engineering Council (Jedec) and in the Rambus and Ramlink architectures (B. Prince, "Memory in the fast lane", IEEE Spectrum, Feb. 1994, pp. 38-41; W. J. Hsieh, "Reconfigurable Hardware", Computer Design, March 1993, pp. 27-30). The key feature in many of these architectures is that the I/O architecture of a RAM is modified so that rapid bursts of data may issue from the internal RAM bus without having to wait

the entire access cycle. RAMs are often built as a square or rectangular array of cells, and the processor first sends a row address and then a column address to specify the cell address. To raise their operating mode, DRAMs have a special operating mode that takes advantage of the internal row-and-column structure, known as the page mode (B. Prince, "Memory in the fast lane", IEEE Spectrum, Feb. 1994, pp. 38-413). In this mode, an entire row is read into the sense amplifiers, the row may be kept active and column addresses changed to access all the data. As long as the accesses remain in the same row, the DRAM can work faster.

The fact that the word width of existing memory chips are fixed, creates a granularity problem in wide-bus memory systems Granularity is the minimum increment of memory that may be added to a system. Personal computers and workstations normally use Single In-line Memory Modules (SIMMs), which are small printed circuit boards stocked with multiple RAM chips arranged in parallel to yield a word width of 32 to 144 bits, matching the memory system word width to the processor's bus width. Hence, memory granularity can sometimes be very troublesome (B. Prince, "Memory in the fast lane", IEEE Spectrum, Feb. 1994, pp. 38-41).

Memory granularity increases as the word width of the memory

chip becomes narrower with respect to the memory bus. Quoting the example used by Prince, in a 16-bit wide bus that uses 4Mb DRAMs, if the chips are organized as 1M X 4 bits, then it takes four of them to fill out the 16-bit memory bus with a minimum granularity of 2 MByte (1 Byte = 8 bits) of memory ((1024 x 1024 x 4)bits/chip x 4 chips ÷ 8bits\Byte = 2 MByte). If, however, the memory chip is organized as 4M X 1 bits, then 16 of them are needed to fill out a 16-bit bus with a minimum granularity of 8 MBytes of memory. The width of the chips used thus affects the expandability of the memory system.

It is desirable to be able to configure the memory chip to a different widths. The only known memory chip that is capable of being reconfigured is the Motorola 1M X 4/2M X 2 bit Fast Static RAM memory chip (Part Number MCM101524). This Motorola chip is a 4Mb RAM whose I/O can be electrically reconfigured from a normal configuration as 1M X 4 bits to 2M X 2 bits by applying power supply voltage to a mode select pin on the chip. Unfortunately, no other reconfigurations are possible.

Therefore, it is an object of this invention to provide an improvement which overcomes the aforementioned inadequacies of the prior art memory chips and provides an improvement which is a significant contribution to the advancement of the memory chip

art.

Another object of this invention is to provide a memory chip of N cells that may be dynamically reconfigured to N X 1 bit, N/2 X 2 bits, N/4 X 4 bits or in general, N/k X k bits, where k is a power of two.

Another object of this invention is to provide a new and useful method for dynamically reconfiguring a computer memory chip of N cells to N X 1 bit, N/2 X 2 bits, N/4 X 4 bits or in general, N/k X k bits, where k is a power of two..

The foregoing has outlined some of the pertinent objects of the invention. These objects should be construed to merely illustrative of some of the more prominent features and applications of the intended invention. Many other beneficial results can be attained by applying the disclosed invention in a different manner or modifying the invention within the scope of the disclosure. Accordingly, other objects and a fuller understanding of the invention made be had by referring to the following summary and the detailed description of the preferred embodiment of the invention, taken in conjunction with the accompanying drawings.

SUMMARY OF THE INVENTION

For the purpose of summarizing this invention, this invention comprises a new and useful computer memory chip, referred to herein as a Field Programmable Memory Cell Array (FPMCA) chip. The FPMCA chip of the invention includes a plurality of memory cells in a predetermined arrangement, a programmable address decoder to enable the memory cells to be addressed and a programmable interconnect having a plurality of programmable connection devices to enable the I/O to be interfaced to a processor. According to one preferred embodiment, the programmable address decoder comprises multiplexers and decoders for addressing the memory cells of the chip and the programmable connection devices comprises PASS transistors for reconfiguring the I/O of the chip.

A method for configuring a computer memory chip, according to the present invention, comprises providing a FPMCA chip as described above, and programming the programmable address decoder and the connection devices as described above so as to reconfigure the arrangement of the memory cells to a selected configuration, and to configure the control logic to interface the memory cells in that selected configuration to a processor in a predetermined manner.

The FPMCA chip of the invention, and the corresponding method for reconfiguring the FPMCA chip, achieves the desired objective of providing a memory chip of N cells that may be dynamically reconfigured to N X 1 bit, N/2 X 2 bits, N/4 X 4 bits or in general, N/k X k bits, where k is a power of two.

The FPMCA chip of the invention will therefore add more flexibility to all uses of memory chips. Memory manufacturers need not make X1, X4, X16 and X32 chips. Only one generic array need be manufactured, and then the generic memory array can be easily programmed to the desired configuration.

Additionally, FPMCA chips of the invention can be used as variable-width memory chips, dynamically configurable caches, dynamically alterable interleaving schemes and other reconfigurable memory architectures.

Accordingly, it should be appreciated that the design of the programmable circuitry allows the use of the FPMCA chip in a variety of different modes since the FPMCA chip can be reconfigured to several different widths and can be interfaced to different processors with different bus widths.

The foregoing has outlined rather broadly the more pertinent and important features of the present invention in order that the detailed description of the invention that follows may be better

understood so that the present contribution to the art can be more fully appreciated. Additional features of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the nature and objects of the invention, reference should be had to the following detailed description taken in connection with the accompanying drawings in which:

Fig. 1 is a block diagram illustrating the organization of a typical memory chip according to the prior art;

Figs. 2A, B and C are block diagrams illustrating the use of a PASS transistor, transmission gate and multiplexer for reconfigurable interconnect according to the prior art;

Fig. 3 is a block diagram illustrating a fully programmable memory cell array according to the present invention in which a sea-of-memory-cells along with a programmable interconnect is present inside the chip;

Fig. 4 is a block diagram illustrating the design of a FPMCA chip according to the present invention, with programmable column decoder and data width;

Fig. 5 is a block diagram illustrating the programmable address decoders of the invention as including demultiplexers and decoders; ;

Fig. 6 is a logic chart illustrating the input and outputs of the control logic in Fig. 5A;

Fig. 7 is a decoding chart illustrating the generation of select signals for the multiplexers of Fig. 5A from three mode pins;

Fig. 8 is a schematic diagram illustrating the programmable connection devices for reconfiguring the I/O width of the FPMCA chip of the invention;

Fig. 9 is a block diagram listing the values for the select signals to the programmable I/O controller for achieving five different configurations of the FPMCA chip of the invention; and

Fig. 10 is a decoding chart illustrating how address pins can be combined with mode pins to minimize the number of necessary pins on the FPMCA chip of the invention.

Similar reference characters refer to similar parts throughout the several views of the drawings.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

As shown in Fig. 1, the field programmable memory cell array (FPMCA) chip 30 of the invention conventionally comprises, as described above, a memory array 12 addressed by a row decoder 14 and a column decoder 16 to input or output data by means of I/O circuits 18 and input and output data control circuits 20 and 22, respectively, as determined by chip select/write enable logic, generally indicated by numeral 24.

The inventive concept of the FPMCA chip 30 of the invention is the inclusion of a programmable address decoder 32 (see Fig. 5) and programmable interconnect 34 (see Fig. 8) that allow selective reconfiguration of the sea of N memory cells 36 (see Fig. 3) of the FPMCA chip 30 to N X 1 bit, N/2 X 2 bits, N/4 X 4 bits or in general, N/k X k bits, where k is a power of two.

Fig. 4 is a block diagram of one embodiment of the FPMCA chip 30 according to the present invention. The FPMCA chip 30 has a hard-wired or rigid row decoder 14 and has a column decoder 16 that comprises the programmable address decoder 32 of the invention. Those skilled in the art will realize that several designs allowing for different levels of programmability in either row or column decoder or both can be realized by incorporating the principles of the present invention.

For purposes of explaining the present invention, a 1M X 1 bit chip is assumed. When the word width is increased to double the existing width, the number of address lines is reduced by one. Thus, when the word width increases k times, the number of address lines gets reduced by log(k). The reconfigurable FPMCA chip 30 supports the number of data pins corresponding to the largest width to be supported and the number address pins corresponding to the smallest width. In the embodiment in Fig. 4, assume that the 1M X 1 bit chip is to be reconfigurable to 512K X 2 bits, or 256K X 4 bits, or 128K X 8 bits, or 64K X 16 bits. In the different configurations, 20, 19, 18, 17, or 16 address pins and 1, 2, 4, 8, 16 data pins respectively, are required. The twenty address pins are designated A0, A1, A2,...A19. The lower 10 address pins A0, A1,...A9 are connected to the row decoder 14. The higher 10 address bits, A10, A11,...A19 are connected to the column decoder 16. The row decoder 14 is hardwired, so it will always have 10 address bits. The column decoder 16 will use 10, 9, 8, 7, and 6 bits when the word width of the chip is 1, 2, 4, 8, and 16 bits respectively.

The purpose of the programmable address decoder 32 and the programmable interconnect 34 is to configure the word width to the desired width and correspondingly configure the column

decoder, column address pins and data pins.

Programmable Address Decoder

The programmable address decoder 32 of the invention comprises four mode control lines 38 (MC1,...MC4) connected to the control inputs 40 of four paired demultiplexers 42 (see Fig. A of Fig. 5 and also Fig. 2C). The data input 44 of one of each paired demultiplexers 42 is respectively connected to the four column address lines 28 (A16,...A19) and the data input 46 of the other of each paired demultiplexers 42 is respectively connected to the complement of such column address lines 28 ($\overline{A}16$,... $\overline{A}19$). The other data inputs 48 of each of the demultiplexers 42 are held high H.

The output terminals 50 (labeled a0, $\overline{a}0$,...a3, $\overline{a}3$ for convenience) of the demultiplexers 42 are logically connected as indicated in Fig. B of Fig. 5 to the enable inputs 52 of sixteen 6X64 decoders 54. The remaining six column address lines 28 (A10,...A15) are respectively connected to the six inputs 56 of the each of the sixteen decoders 54. The 1024 outputs 58 of the sixteen 6X64 decoders 54 (16 x 64 = 1024) are respectively connected to the columns 36C of the memory array 12.

It is noted that since there are sixteen 6X64 decoders 54 and since they are enabled depending upon the logic state of the

four mode control lines 38, only 1, 2, 4, 8 or 16 of such decoders 54 will be enabled at any one time. Further, since only one of the outputs 58 of the enabled decoders 56 may will high depending upon the respective inputs 56, only 1, 2, 4, 8, or 16 columns 36C of the memory array 12 are addressed. With 1, 2, 4, 8, or 16 columns of the memory cells 36 being addressed, the word length of the FPMCA chip 30 may be 1, 2, 4, 8, or 16 bits wide (see the logic table of Fig. 6).

Since there are five different modes to be supported, at least three external mode pins are required for mode control. More specifically, as shown in the logic table of Fig. 7, the three external mode pins (M1, M2, M3) may be translated by suitable logic 60 (see Fig. 5), to the four mode control lines (MC1, MC2, MC3, MC4).

<u>Programmable Interconnect</u>

Referring now to Fig. 8, the output circuitry of the 16-bit wide FPMCA chip can be programmed to 8, or 4, or 2, or 1 bit word widths by means of a PASS transistors 62 (see Fig. 2A) or a transmission gate 64 (see Fig. 2B), or other suitable switch. More particularly, PASS transistors 62 are placed between the data lines 66 of the I/O circuits of the FPMCA chip 30 so that they can be connected together or not, depending on the desired

word width. As illustrated, four levels of PASS transistors are required to change the word width to include 1, 2, 4, 8 and 16 widths.

In general, log(k) levels of PASS transistors 62 are required for varying the word width to k times. In fact, all of the PASS transistors 62 in any one level will be having identical contents. This principle may be used to reduce the number of mode control lines used in the circuit. The PASS transistors 62 can be programmed to the aforementioned level of flexibility by log(k) control lines, one for each level of PASS transistors 62.

Fig. 8 illustrates the manner in which sixteen data lines 66 can be controlled by the four mode control lines 38 (described above in connection with the programmable address decoder 32) to yield any word width from 16, 8, 4, 2 to 1, which are powers of two. Fig. 9 illustrates the values required to control the PASS transistors 62. It is noted that a circuit similar to Fig. 8 has to be incorporated into the input circuitry also. The mode control lines 38 controlling the PASS transistors in the input data lines can be the same as those in the output circuitry.

At this point it is noted that the mode control lines 38 for the programmable address decoder 32 has identical values as the mode control lines for word-width adjustment and hence the same

lines may be used. The mode control lines could be replaced by a mode control register built of static RAM cells (as in Xilinx FPGAs). In an embodiment that uses the static RAM cells to control the chip width, the values in the static RAM cells will correspond to Fig. 9.

Looking at the values on the mode control lines 38 as in Fig. 9, it can be seen that out of the 16 possible values for the 4 mode control lines, only 5 are being used. In general, out of all possible k combinations of contents for the log(k) select lines, only log(k) + 1 combinations are being used. Hence the number of control lines may be minimized to log (log(k) + 1). Thus just 3 lines are sufficient for programming from 1 bit to 16 bit. From 3 lines, the four control signals can be generated according to Fig. 7. Even in a case for programming from 1 bit to 1024 bit width, all that is required is 4 lines.

Finally, as shown in Fig. 10, the log (log(k) + 1) lines or 4 control lines in the embodiment in Fig. 4 can be overlapped with the address bits. Specifically, each increase in the data width by k times, reduces the number of address lines required by log(k). Those lines can be shared to deliver the mode information to the chip. Fig. 10 illustrates the manner in which the address lines and the mode control bits can be shared. Only

one extra line will be required to indicate the mode. That line if 0 commands the chip to be in the narrowest possible configuration. If the line is 1, the chip is in a wider mode. Hence at least the highest address line A20 is not required for addressing. So A20 can be used for mode information. If A20 is 0, the chip is twice as wide as the narrowest configuration. If A20 is a 1, the chip is even wider. So A19 is not required for addressing and will be used for mode information. If A19 is 0, the chip is 4 times as wide as the narrowest configuration. If A19 is 1, the chip is wider than 4 times the original width. So A18 will not be required for addressing and can be used for mode information. If A18 is a 0, the chip is 8 times the original width and if A18 is a 1, the chip is 16 times the original width. Thus mode control can be accomplished by just one extra pin. Even that one pin can be overlapped with some of the data pins.

The present disclosure includes that contained in the appended claims, as well as that of the foregoing description. Although this invention has been described in its preferred form with a certain degree of particularity, it is understood that the present disclosure of the preferred form has been made only by way of example and that numerous changes in the details of construction and the combination and arrangement of parts may be

resorted to without departing from the spirit and scope of the invention.

Now that the invention has been described,

WHAT IS CLAIMED IS:

1. A computer memory chip comprising

(i) a plurality of memory cells in a predetermined arrangement,

(ii) a plurality of programmable connection devices at selected locations in the memory chip, and

(iii) programmable control logic to enable the memory cells to be addressed and interfaced to a data processing device,

whereby the width of the memory chip may be reconfigured.

2. A computer memory chip as set forth in claim 1, wherein said programmable connection devices comprise PASS transistors.

3. A computer memory chip as set forth in claim 1, wherein said programmable connection devices comprise multiplexers.

4. A method for configuring a computer memory chip, comprising the steps of

(a) providing a computer memory chip with

(i) a plurality of memory cells in a predetermined arrangement

(ii) a plurality of programmable connection devices at selected locations in the memory chip, and

(iii) programmable control logic to enable the memory cells to be addressed and interfaced to a data processing device, and

(b) programming selected programmable connection devices to reconfigure the arrangement of the memory cells to a selected configuration, and to configure the control logic to interface the memory cells in that selected configuration to a data processing device in a predetermined manner.

5. A method as set forth in claim 4, wherein the step of programming selected memory devices is adapted to reconfigure the width of the memory chip.

6. A field programmable memory cell array, comprising in combination:

a plurality of memory cells in a predetermined arrangement including input and output;

a programmable address decoder for enabling addressing of said memory cells; and

a programmable I/O controller for interfacing said input and output of said plurality of memory cells.

7. The array as set forth in Claim 6, wherein said programmable address decoder comprises multiplexers and decoders for addressing said memory cells and wherein said programmable I/O controller comprises switch means for reconfiguring said input and output.

8. A method for configuring the array of Claim 6, comprising the steps of programming said programmable address decoder and said programmable I/O controller to reconfigure said arrangement of memory cells to a selected configuration and to configure said control logic to interface said memory cells in said selected configuration.

9. The array as set forth in Claim 6, wherein said array is configured as a variable-width memory device.

10. The array as set forth in Claim 6, wherein said array is configured as a dynamically configurable cache device.

11. The array as set forth in Claim 6, wherein said array is configured as a reconfigurable memory device.

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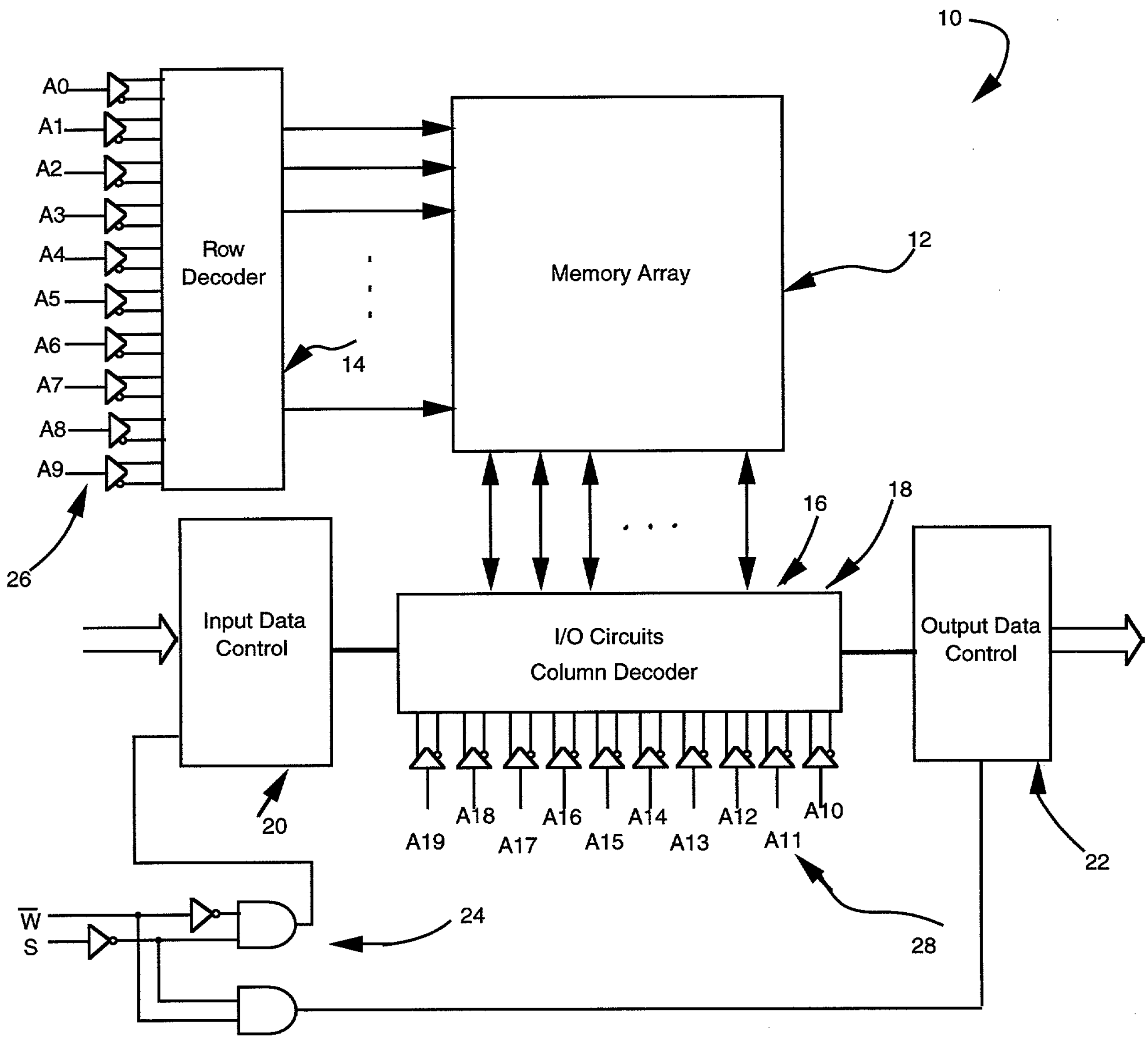

FIG. 1

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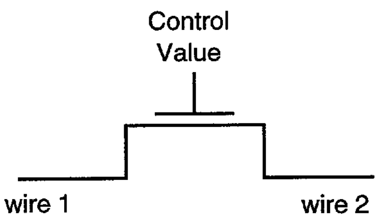

FIG 2A

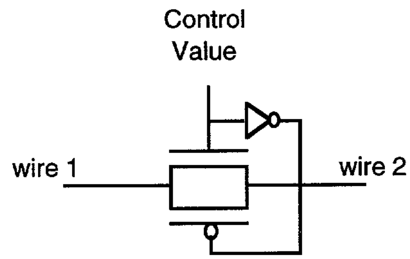

FIG 2B

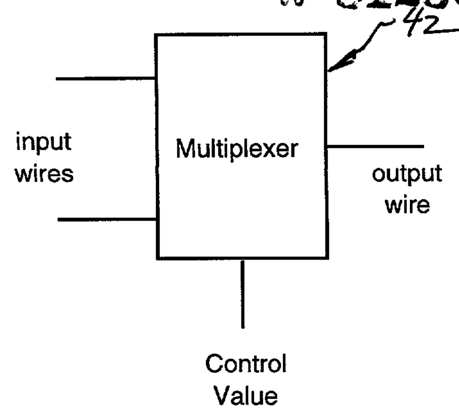

FIG 2C

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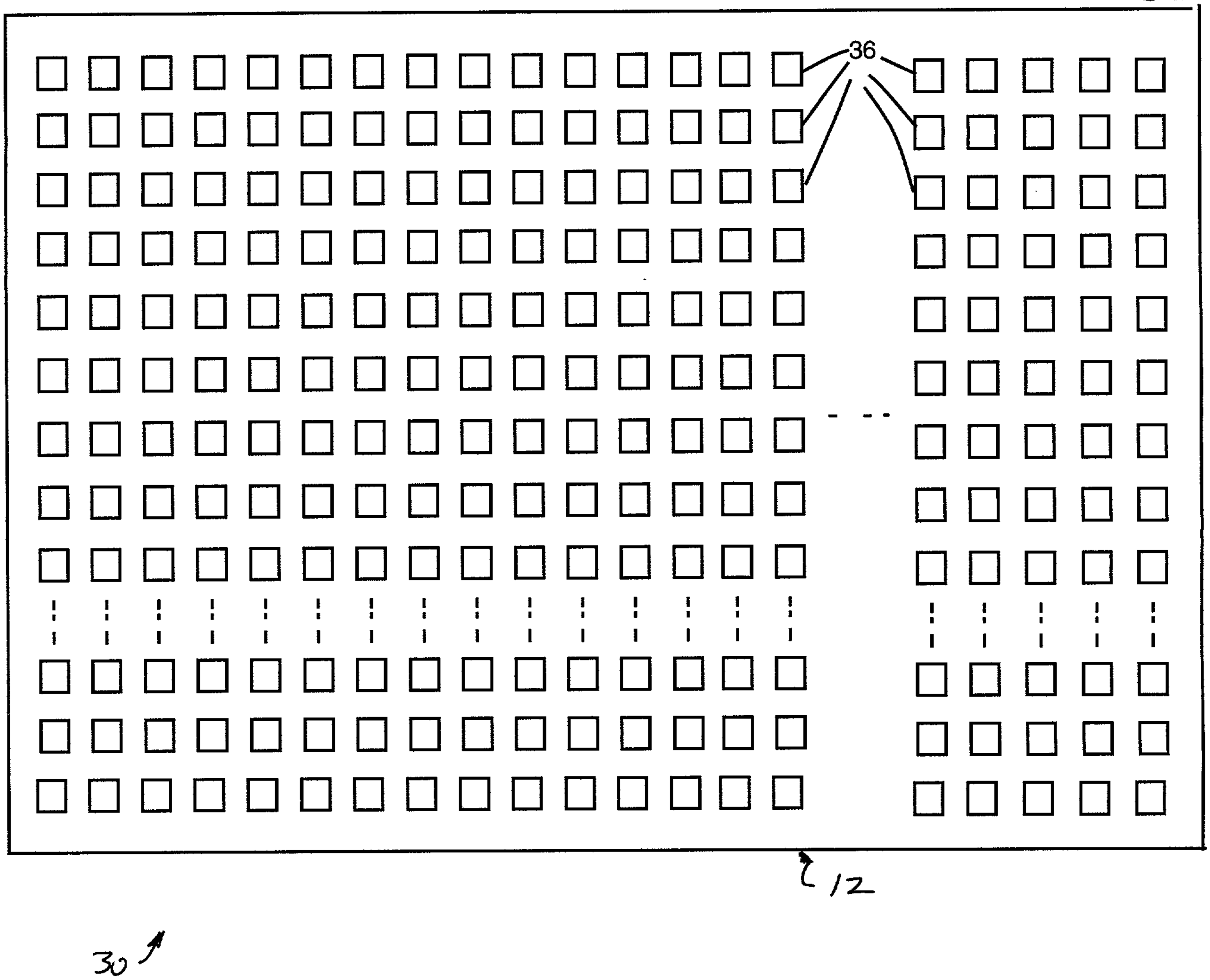

FIG. 3

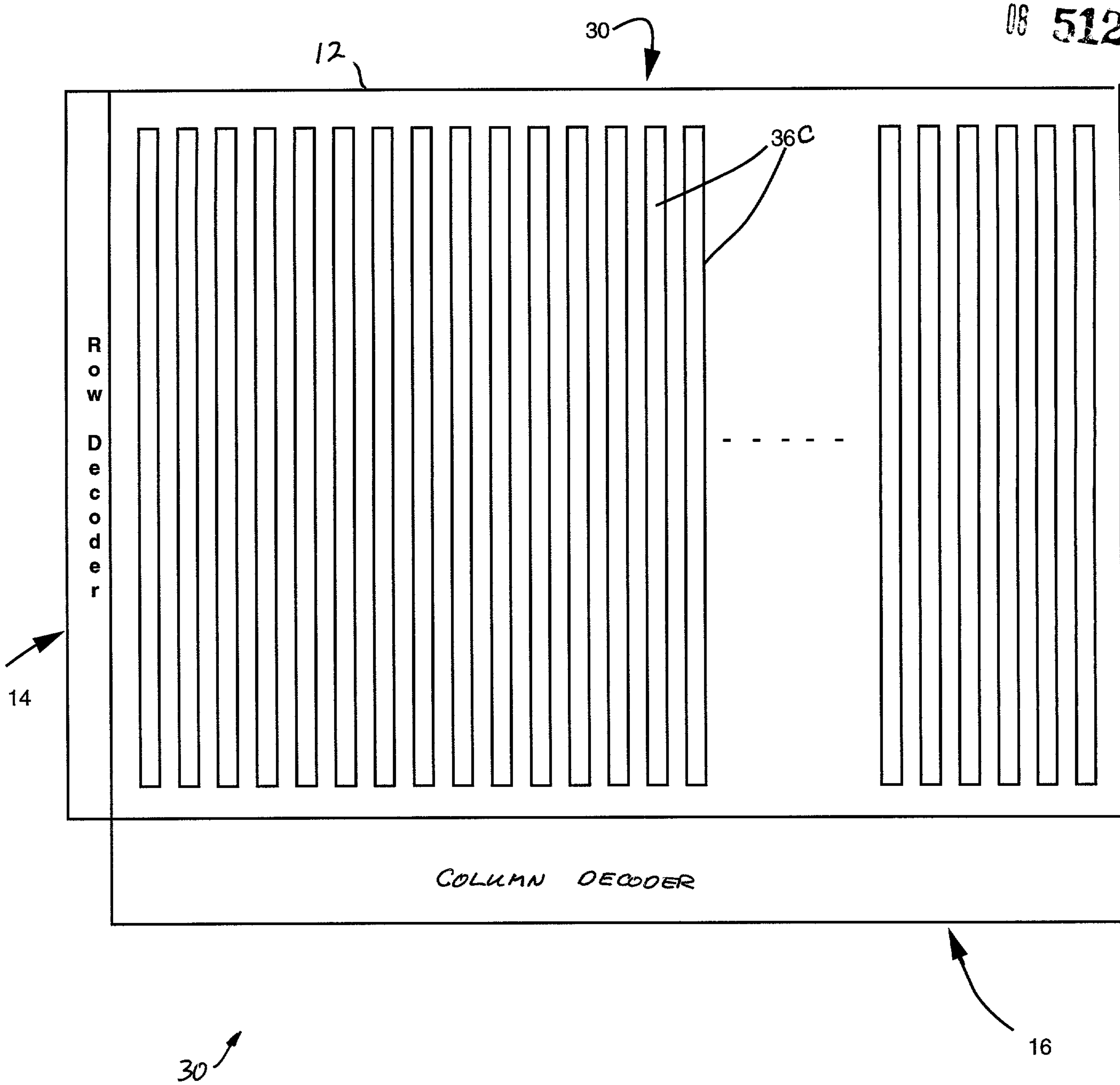

FIG 4

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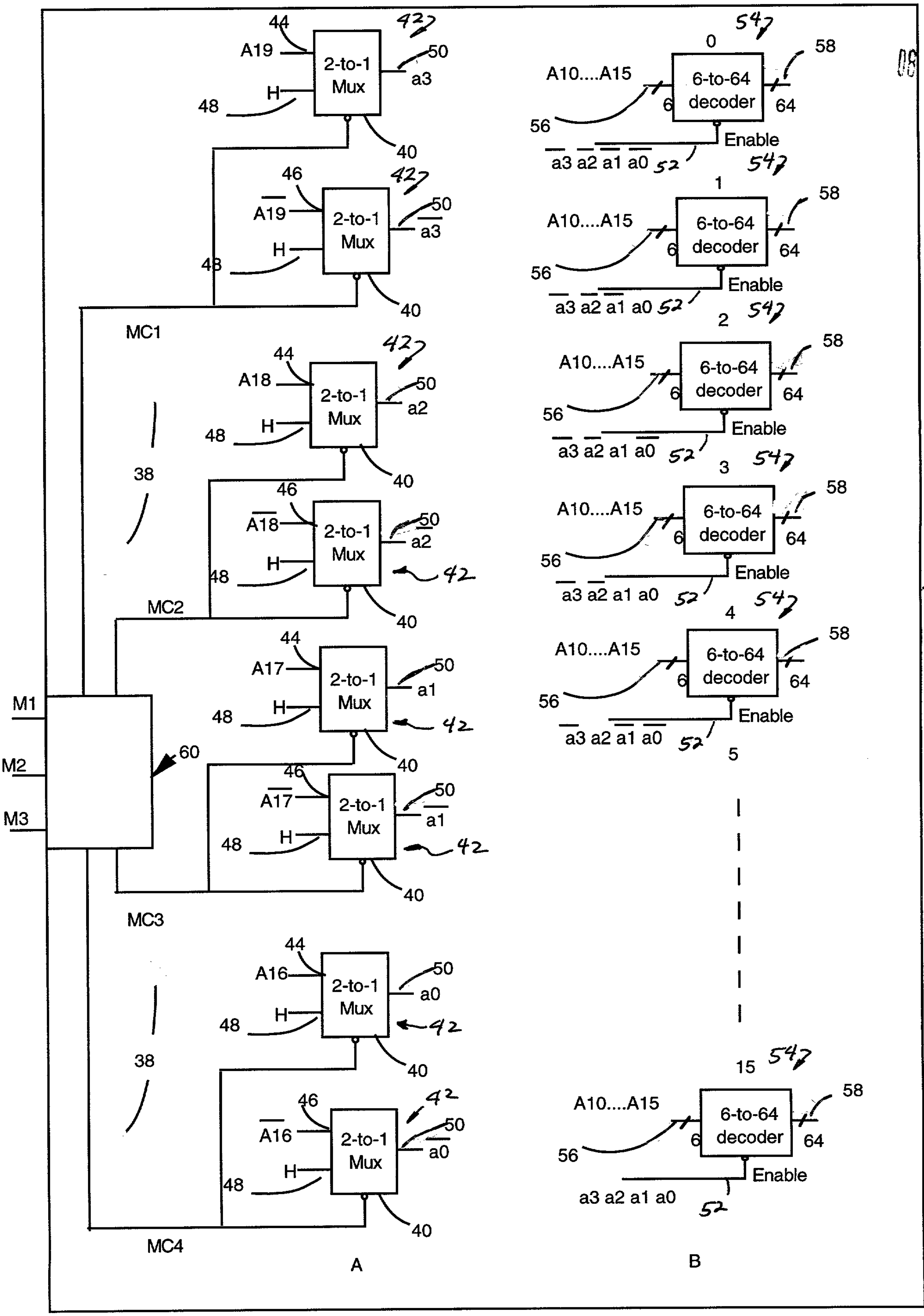

FIG 5

MC4	MC3	MC2	MC1	a3	a2	a1	a0	$\overline{a3}$	$\overline{a2}$	$\overline{a1}$	$\overline{a0}$	Configuration
1	1	1	1	A19	A18	A17	A16	$\overline{A19}$	$\overline{A18}$	$\overline{A17}$	$\overline{A16}$	1 bit wide
1	1	1	0	H	A18	A17	A16	H	$\overline{A18}$	$\overline{A17}$	$\overline{A16}$	2 bit wide
1	1	0	0	H	H	A17	A16	H	H	$\overline{A17}$	$\overline{A16}$	4 bit wide
1	0	0	0	H	H	H	A16	H	H	H	$\overline{A16}$	8 bit wide
0	0	0	0	H	H	H	H	H	H	H	H	16 bit wide

FIG. 6

M3	M2	M1	MC4	MC3	MC2	MC1
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	1	1	0	0
0	1	1	1	1	1	0
1	0	0	1	1	1	1

FIG 7

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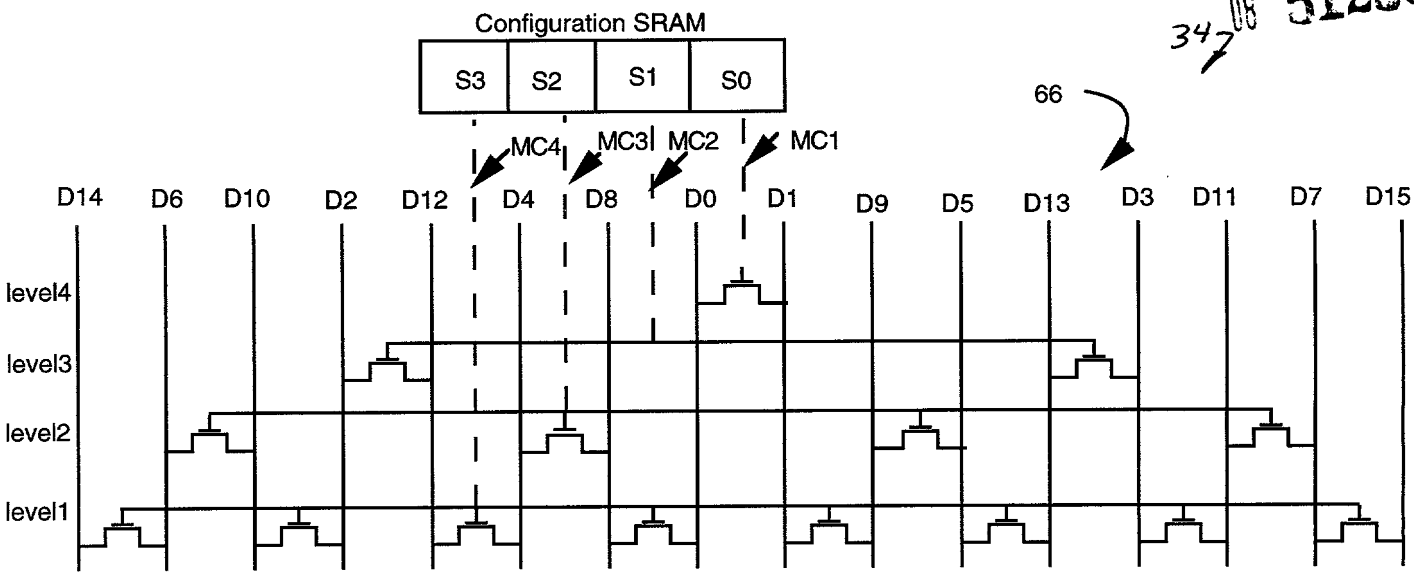

FIG 8

Configuration RAM contents				Resulting Configuration
0	0	0	0	16 bit wide
1	0	0	0	8 bit wide
1	1	0	0	4 bit wide
1	1	1	0	2 bit wide
1	1	1	1	1 bit wide
S3	S2	S1	S0	

FIG. 9

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M	A19	A18	A17	A16	MC4	MC3	MC2	MC1	Configuration
0	x	x	x	x	1	1	1	1	1 bit wide
1	0	x	x	x	1	1	1	0	2 bit wide
1	1	0	x	x	1	1	0	0	4 bit wide
1	1	1	0	x	1	0	0	0	8 bit wide
1	1	1	1	x	0	0	0	0	16 bit wide

FIG. 10

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Lizy Kurian John

SERIAL NUMBER: 08/512,505

FILED: August 8, 1995

FOR: COMPUTER MEMORY CHIP WITH FIELD PROGRAMMABLE MEMORY CELL ARRAYS (FPMCAs) AND METHOD OF CONFIGURING

ATTORNEY DOCKET NO.: 2115.007

DECLARATION FOR PATENT APPLICATION

As below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe that I am an original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled Computer Memory Chip With Field Programmable Memory Cell Arrays (FPMCAs) and Method of Configuring, Serial Number 08/512,505, the specification of which was filed August 8, 1995;

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, section 1.56(a).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Lizy Kurian John

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FILED: August 8, 1995

FOR: COMPUTER MEMORY CHIP WITH FIELD PROGRAMMABLE MEMORY CELL ARRAYS (FPMCAs) AND METHOD OF CONFIGURING

ATTORNEY DOCKET NO.: 2115.007

POWER OF ATTORNEY

University of South Florida, Applicant's complete assignee, does hereby appoint Stefan V. Stein, Registration No. 29,702, Leon Chasan, Registration Number 15,970, Stephan A. Pendorf, Registration No. 32,665, and John J. Snyder, Registration Number 39,380, as their attorneys in the above entitled application, with full power of substitution, association and revocation, to transact all business in the United States Patent and Trademark Office connected therewith.

Further, please send all correspondence to:

Stefan V. Stein
Suite 1000
600 N. Westshore Blvd.
Tampa, Florida 33609

Direct all telephone calls to Stefan V. Stein at:

(813) 289-2966.

EXECUTED by me on this the 4 day of October, 1995, at Tampa, Hillsborough County, Florida.

[signature]

By: RG Preston

Its: Ass't Vice President for Research

08512505.080595

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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FOR: COMPUTER MEMORY CHIP WITH FIELD PROGRAMMABLE MEMORY CELL ARRAYS (FPMCAs) AND METHOD OF CONFIGURING

ATTORNEY DOCKET NO.: 2115.007

VERIFIED STATEMENT CLAIMING SMALL ENTITY STATUS
INDEPENDENT INVENTOR

As below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled Wafer Shielding Chamber for Probe Station, described in the specification filed herewith.

I have not assigned, granted, conveyed or licensed nor am I under an obligation under contract or law to assign, grant, convey, or license any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a

nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below and a verified statement from each averring to their status as a small entity is attached hereto.

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Tampa, Florida 33620
NonProfit Organization

I acknowledge the duty to file, in this application, notification or any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; that I have read this Affidavit and know the contents thereof; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such

willful false statements may jeopardize the validity of the application or any patent issued thereon.

Lizy Kurian John

Lizy Kurian John

Date: 09/28, 1995

Computer Memory Chip with Field Programmable Memory Cell Arrays (FPMCAs) and Method of Configuring

Dominick & Stein

Docket No. 2115.007

VERIFIED STATEMENT CLAIMING SMALL ENTITY STATUS
37 C.F.R. 1.9(f) AND 1.27(d)
NON-PROFIT ORGANIZATION

I hereby declare that I, George R. Newkome, Ph.D., am an officer empowered to act on behalf of the University of South Florida, 4202 East Fowler Avenue, ADM #200, Tampa, Florida 33620.

TYPE OF ORGANIZATION:

_x_ University or other institution of higher education.

____ Tax exempted under Internal Revenue Service Code (26 U.S.C. §501(a) and §501(c)(3)).

____ Non-profit scientific or educational under statute of state of the United States of America.
(Name of State __________)
(Citation of statute)

____ Would qualify as tax exempt under Internal Revenue Code (26 U.S.C. §501(a) and §501(c)(3)) if located in the United States of America.

____ Would qualify as a non-profit scientific or educational under statute of the state of the United States of America if located in the United States of America.
(Name of State __________)
(Citation of statute)

I hereby declare that the non-profit organization identified above qualifies as a non-profit organization as defined in 37 C.F.R. 1.9(e) for purposes of paying reduced fees under §41(a) and §41(b) of Title 35, United States Code with regard to the invention entitled

COMPUTER MEMORY CHIP WITH FIELD PROGRAMMABLE MEMORY CELL ARRAYS (FPMCAs) AND METHOD OF CONFIGURING

by inventor **LIZY KURIAN JOHN** described in

____ the specification filed herewith.

_x_ application serial number 08/512,505, filed on August 8, 1995.

____ patent number ________________, issued ________________.

I hereby declare that the rights under contract or law have been conveyed to and remain with the non-profit organization regarding the above identified invention. If the rights held by the non-profit organization are not exclusive, each individual, concern or organization having rights in the invention must file separate verified statements averring to their status as small entities and that no rights to the

invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 C.F.R. 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 C.F.R. 1.9(d) or a non-profit organization under 37 C.F.R. 1.9(e).

Each person, concern or organization having any rights in the invention is listed below:

____ no such person exists.

_x_ each such person, concern or organization is listed below.

UNIVERSITY OF SOUTH FLORIDA
4202 East Fowler Ave., FAO 126
Tampa, Florida 33620-4962

UNIVERSITY OF SOUTH FLORIDA RESEARCH FOUNDATION, INC.
4202 East Fowler Ave., FAO 126
Tampa, Florida 33620-4962

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate (37 C.F.R. 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

UNIVERSITY OF SOUTH FLORIDA

Date: 10/4/95

By: [signature]
George R. Newkome, Ph.D.
Vice President for Research
University of South Florida
4202 East Fowler Ave., FAO 126
Tampa, Florida 33620-4962